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ABSTRACT OF THE DISCLOSURE

An image processing apparatus provides numerical signal generator for sequentially generating and outputting regular binary numerical signals synchronous with clock signal, bit exchanger for generating and outputting, from the output signal of the numerical signal generator being managed as input signal, signal that order of bits in the input signal has been exchanged or signal that the bits in the input signal have been reversed, controller for controlling the bit order exchange operation or the bit reversal operation of the bit exchanger, and storage for storing image data, and in the apparatus the image data divided into pixel data and one-dimensionally arranged and stored in the storage is read and output synchronous with the sequential operation of the numerical signal generator, and the output signal from the bit exchanger is read and output as address signal to perform rotation/reversal process to former image.